

a reset transistor for resetting said pixel;
an amplifier having:
 a first input for receiving said outputs of said pixels, and
 an output coupled to said reset transistors to provide a
 negative feedback signal to a selected pixel; and
a reset reference voltage source connected to apply a reset reference
signal to said amplifier to provide a voltage reference for controlling reset
pixels.

2. (Amended) The image sensor of claim 1 wherein said amplifier further includes a second input receiving said reset reference voltage signal.

3. (Amended) The image sensor of claim 2 wherein said reset transistor includes a gate and first and second terminals, said first terminal connected to receive said negative feedback signal to adjust said second terminal's voltage to a selected reset voltage.

4. (Amended) The image sensor of claim 3 wherein said reset reference voltage source signal is selected to control said voltage at said second reset transistor terminal to be about $V_T - \Delta V$ below a reset voltage applied at said gate terminal of said reset transistor, where V_T is a threshold voltage that is characteristic of said reset transistor, and ΔV is selected to maintain said reset transistor in a subthreshold region of operation during a steady state phase of pixel reset.

5. (Amended) The image sensor of claim 4 wherein said selected ΔV is greater than about one hundred millivolts.

1 6. (Amended) The image sensor of claim 4 wherein said select node of
2 each said pixel comprises a terminal of a row select transistor that is coupled to
3 said first input of said amplifier.

1 7. (Amended) The image sensor of claim 6 wherein each said pixel further
2 comprises a source follower transistor coupled between said second terminal of
3 said reset transistor and a terminal of said row select transistor.

1 8. (Amended) The image sensor of claim 3 wherein said first circuit
2 comprises a photocircuit.

1 9. (Amended) The image sensor of claim 8 wherein said amplifier
2 comprises a differential amplifier including a first differential amplifier input
3 transistor connected to receive said first amplifier input and a second differential
4 amplifier input transistor connected to receive said second amplifier input, said
5 first and second differential amplifier input transistors connected to provide a
6 signal to a current mirror circuit that is connected to deliver said negative feedback
7 signal to said reset transistor first terminal.

1 10. (Amended) The image sensor of claim 8 wherein said photocircuit
2 includes a photodiode and a capacitance.

1 11. (Amended) The image sensor of claim 7 wherein said first circuit is a
2 photocircuit.

1 12. (Amended) The image sensor of claim 11 wherein said photocircuit
2 includes a photodiode and a capacitance.

*AI
CONT.*

1 13. (Amended) An image sensor array having rows and columns of pixels,
2 comprising:

3 at least one column line;
4 a plurality of pixels each having an output, the outputs of pixels in a
5 column being connected to a common respective column line, each said pixel
6 including:

7 a first circuit that produces a signal proportional to incident
8 light intensity, said first circuit being connected to supply said
9 proportional signal to said pixel output, and
10 a reset transistor for resetting said pixel;

11 at least one amplifier, each said amplifier having a first input coupled to at
12 least one said column line, each said amplifier being connected to provide a
13 negative feedback signal to each said pixel reset transistor of a respective column
14 of pixels; and

15 a reset reference voltage source connected to apply a reset reference voltage
16 signal to each said amplifier to provide a voltage reference for controlling reset of
17 said pixels.

1 14. (Amended) The image sensor of claim 13 wherein said amplifier
2 further includes a second input for receiving said reset reference voltage signal.

1 15. (Amended) The image sensor of claim 14 wherein said reset transistor
2 includes a gate and first and second terminals, said first terminal connected to
3 receive said negative feedback signal to adjust said second terminal's voltage to a
4 selected reset voltage.

1 16. (Amended) The image sensor of claim 15 wherein said reset reference
2 voltage source signal is selected to control said voltage at said second reset

3 transistor terminal to be about $V_T - \Delta V$ below a reset voltage applied at said gate
4 terminal of said reset transistor, where V_T is a threshold voltage that is
5 characteristic of said reset transistor, and ΔV is selected to maintain said reset
6 transistor in a subthreshold region of operation during a steady state phase of pixel
7 reset.

1 17. (Amended) The image sensor array of claim 15 wherein said selected
2 ¹⁶
 ΔV is greater than about one hundred millivolts.

1 18. (Amended) The image sensor array of claim 16 wherein each pixel
2 comprises a row select transistor coupled between said second terminal of said
3 reset transistor and said first input of said amplifier.
4

5 19. (Amended) The image sensor array of claim 18 wherein each pixel
6 further comprises a source follower transistor coupled between said second
7 terminal of said reset transistor and a terminal of said row select transistor.

1 20. (Amended) The image sensor array of claim 16 wherein said first
2 circuit of each pixel comprises a photocircuit.

1 21. (Amended) The image sensor array of claim 20 wherein said amplifier
2 comprises a differential amplifier including a first differential amplifier input
3 transistor connected to receive said first amplifier input and a second differential
4 amplifier input transistor connected to receive said second amplifier input, said
5 first and second differential amplifier input transistors connected to provide a
6 signal to a current mirror circuit that is connected to deliver said negative feedback
7 signal to said reset transistor first terminal.

*A1
CON*

1 22. (Amended) The image sensor array of claim 20 wherein said
2 photocircuit of each active pixel comprises a photodiode and a capacitance.

1 23. (Amended) The image sensor array of claim 19 wherein each said first
2 circuit comprises a photocircuit.

1 24. (Amended) The image sensor array of claim 23 wherein each said
2 photocircuit comprises a photodiode and a capacitance.

1 25. (Amended) ~~An~~ image sensor array having rows and columns of pixels,
2 comprising:

3 at least one row line;

4 a plurality of pixels each having an output, the outputs of pixels in a row
5 being connected to a common respective row line, each said pixel including:

6 a first circuit that produces a current proportional to incident

7 light intensity, said first circuit being connected to supply said

8 proportional current to said pixel output, and

9 a reset transistor for resetting said pixel;

10 at least one amplifier, each said amplifier having a first input coupled to at
11 least one said row line, each said amplifier being connected to provide a negative
12 feedback signal to each said pixel reset transistor of a respective row if pixels; and

13 a reset reference voltage source connected to apply a reset reference voltage
14 signal to each said amplifier to provide a voltage reference for controlling reset of
15 said pixels.

1 26. (Amended) The image sensor of claim 25 wherein said amplifier
2 further includes a second input for receiving said reset reference voltage signal.

AI
CONT.

1 27. (Amended) The image sensor of claim 26 wherein said reset transistor
2 includes a gate and first and second terminals, said first terminal connected to
3 receive said negative feedback signal to adjust said second terminal's voltage to a
4 selected reset voltage.

1 28. (Amended) The CMOS image sensor of claim 27 wherein said reset
2 reference voltage source signal is selected to control said voltage at said second
3 terminal to be about $V_T - \Delta V$ below a reset voltage applied at said gate terminal of
4 said reset transistor, where V_T is a threshold voltage that is characteristic of said
5 reset transistor, and ΔV is selected to maintain said reset transistor in a
6 subthreshold region of operation during a steady state phase of pixel reset.

1 29. (Amended) The image sensor array of claim 27 wherein said selected
2 ΔV is greater than about one hundred millivolts. ²⁸

1 30. (Amended) The image sensor array of claim 28 wherein each pixel
2 comprises a column select transistor coupled between said second terminal of said
3 reset transistor and said first input of said amplifier.

1 31. (Amended) The image sensor array of claim 30 wherein each pixel
2 further comprises a source follower transistor coupled between said second
3 terminal of said reset transistor and a terminal of said column select transistor.

1 32. (Amended) The image sensor array of claim 28 wherein said first
2 circuit of each pixel comprises a photocircuit.

1 33. (Amended) The image sensor array of claim 32 wherein said amplifier
2 comprises a differential amplifier including a first differential amplifier input

*AI
unc/c*

3 transistor connected to receive said first amplifier input and a second differential
4 amplifier input transistor connected to receive said second amplifier input, said
5 first and second differential amplifier input transistors connected to provide a
6 signal to a current mirror circuit that is connected to deliver said negative feedback
7 signal to said reset transistor first terminal.

1 34. (Amended) The image sensor array of claim 32 wherein said
2 photocircuit of each pixel comprises a photodiode and a capacitance.

1 35. (Amended) The image sensor array of claim 31 wherein each said first
2 circuit comprises a photocircuit.

1 36. (Amended) The image sensor array of claim 35 wherein each said
2 photocircuit comprises a photodiode and a capacitance.

A2

1 37. (New) The image sensor of claim 1 wherein said image sensor
2 comprises a CMOS-compatible image sensor.

1 38. (New) The image sensor array of either of claims 13 or 25 wherein said
2 image sensor array comprises a CMOS-compatible image sensor array.

1 39. (New) The image sensor of claim 1 wherein said pixels comprise active
2 pixels.

1 40. (New) The image sensor array or either of claims 13 or 25 wherein
2 said pixels comprise active pixels.